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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,417	03/02/2004	Wan Yen Teoh	03-11	5407

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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,417	TEOH ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed July 17, 2006 in response to the Office action dated May 2, 206. Claims 1, 4-6, 9-11, 14-17, and 20 have been amended. Claims 1-20 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendment, the objections to the specification have been withdrawn.

Claims

2. In view of Applicant's amendment, the objection to **claim 17** has been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 7-9, 11-15, and 17-19 are rejected under 35 U.S.C. 103(a) as being obvious over So (U.S. Patent 5,883,844) in view of Okazawa (U.S. Patent 6,308,249).

5. **As per claim 1**, So discloses a method of testing a memory device for determining operating life with stressing, comprising:

cycling through each address of the memory device by generating a respective bit pattern comprised of a predetermined number of bits for each address (col. 6, lines 5-14; Fig. 3, elements 33 and 37); *It should be noted that the "boundaries between only two adjacent rows R and only two adjacent columns C of the memory block" are analogous to the "memory device."*

applying stressing signals on a respective at least one cell of the memory device corresponding to each generated address in the cycling (col. 5, lines 39-46 and 56-60; Fig. 3, elements 30 and 31). *It should be noted that the "high frequency waveform" is analogous to the "stressing signal."*

performing the cycling and the applying of the stressing signals for a predetermined stress time period (col. 4, line 66 – col. 5, line 7).

So does not expressly disclose minimizing charge gain failure in the memory device after the predetermined stress time period with a translation of less than the predetermined number of bits for sequencing to each subsequent address during the cycling.

Okazawa discloses minimizing charge gain failure in the memory device after the predetermined stress time period with a translation of less than the predetermined

number of bits for sequencing to each subsequent address during the cycling (col. 5, lines 24-39 and 53-67; Fig. 3; Fig. 4). *It should be noted that when taking the broadest reasonable interpretation of the claim language Okazawa uses a small number of bit transitions for going to a subsequent address in cycling through each address of a memory device and therefore discloses "minimizing" charge gain failure. It should also be noted that when taken in combination with So, Okazawa's translation occurs after So's predetermined stress time period. Finally, it should be noted that "accessing" is analogous to "cycling" and that Okazawa's grey code bit pattern requires only 16 bit transitions when accessing proceeds consecutively from the 1st address to the 32nd address as opposed to the binary bit pattern (i.e. the pattern that sequences to each subsequent address) which requires 32 bit transitions when accessing proceeds consecutively from the 1st address to the 32nd address.*

So and Okazawa are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Okazawa's grey code bit pattern into So's testing patterns.

The motivation for doing so would have been to reduce switching activity (i.e. increase speed) by minimizing bit transitions when using gray code addressing as opposed to binary code addressing.

Therefore, it would have been obvious to combine So and Okazawa for the benefit of obtaining the invention as specified in claim 1.

6. **As per claim 2**, the combination of So/Okazawa discloses cycling through the respective bit pattern for each of the addresses in a gray code sequence (Okazawa, col. 5, lines 9-17). *It should be noted that "grey code" is equivalent to "gray code."*

7. **As per claim 3**, the combination of So/Okazawa discloses the memory device is a flash memory device (So, col. 3, lines 51-55).

8. **As per claim 4**, the combination of So/Okazawa discloses the stressing signals include a clock signal applied on a respective word line corresponding to each generated address, and include a bit line voltage applied on a respective at least one bit line corresponding to each generated address (So, col. 4, lines 52-59; col. 5, lines 7-12, 39-46, and 56-60; Fig. 1, element 16; Fig. 3, element 31). *It should be noted that the "high frequency waveform" is also analogous to the "bit line voltage."*

9. **As per claim 5**, the combination of So/Okazawa discloses generating a respective binary bit pattern for each of the addresses (Okazawa, col. 3, lines 35-37; Fig. 1, element 1);

converting the respective binary bit pattern to a respective gray code bit pattern for each of the addresses (Okazawa, col. 3, lines 39-44; Fig. 1, element 2);

and using the respective gray code bit pattern for the cycling (Okazawa, col. 3, lines 44-46; col. 5, lines 24-39 and 53-67). *See citation note for the similar limitation in claim 1 above.*

10. **As per claim 7**, the combination of So/Okazawa discloses cycling through the respective bit pattern for each of the addresses with a transition of a fixed number of bits for sequencing to each subsequent address (Okazawa, col. 5, lines 53-67; Fig. 4).

It should be noted as indicated by Fig. 4 the grey code bit pattern has a fixed number of bit transitions for sequencing to each subsequent address (that fixed number being 1).

11. **As per claim 8**, the combination of So/Okazawa discloses the memory device is a flash memory device (So, col. 3, lines 51-55).

12. **As per claim 9**, the combination of So/Okazawa discloses the stressing signals include a clock signal applied on a respective word line corresponding to each generated address, and include a bit line voltage applied on a respective at least one bit line corresponding to each generated address (So, col. 4, lines 52-59; col. 5, lines 7-12, 39-46, and 56-60; Fig. 1, element 16). *See the citation note for claim 9 above.*

13. **As per claim 11**, So discloses a method of testing a memory device for determining operating life with stressing, comprising:

an address generator for cycling through each address by generating a respective bit pattern comprised of a predetermined number of bits for each address (col. 6, lines 5-14; Fig. 3, elements 33 and 37); *It should be noted that the "test pattern generating means" is analogous to the "address generator."*

signal generators for generating stressing signals applied on a respective at least one cell of the memory device corresponding to each generated address in the cycling (col. 5, lines 39-46 and 56-60; Fig. 3, elements 30 and 31). *It should be noted that the "the stress testing means" is analogous to the "signal generators." Also, see the citation note for the similar limitation in claim 1 above.*

wherein the cycling and the applying of the stressing signals for a predetermined stress time period (col. 4, line 66 – col. 5, line 7).

So does not expressly disclose means for minimizing charge gain failure in the memory device after the predetermined stress time period with a translation of less than the predetermined number of bits for sequencing to each subsequent address during the cycling.

Okazawa discloses means minimizing charge gain failure in the memory device after the predetermined stress time period with a translation of less than the predetermined number of bits for sequencing to each subsequent address during the cycling (col. 5, lines 24-39 and 53-67; Fig. 3; Fig. 4). *It should be noted that pg. 12, lines 27-29 of Applicant's specification appear to define this means as a "binary to gray code converter." Okazawa's "binary/grey conversion logic circuit" is equivalent to Applicant's "binary to gray code converter." Also, see the citation note for the similar limitation in claim 1 above.*

So and Okazawa are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Okazawa's grey code bit pattern into So's testing patterns.

The motivation for doing so would have been to reduce switching activity (i.e. increase speed) by minimizing bit transitions when using gray code addressing as opposed to binary code addressing.

Therefore, it would have been obvious to combine So and Okazawa for the benefit of obtaining the invention as specified in claim 11.

14. **As per claim 12**, the combination of So/Okazawa discloses a gray code converter for cycling through the respective bit pattern for each of the addresses in a gray code sequence (Okazawa, col. 5, lines 9-17). *It should be noted that "binary/grey conversion logic circuit" is analogous to "gray code converter." Also, see the citation note for claim 2 above.*

15. **As per claim 13**, the combination of So/Okazawa discloses the memory device is a flash memory device (So, col. 3, lines 51-55).

16. **As per claim 14**, the combination of So/Okazawa discloses the signal generators include:

a clock signal generator for generating a clock signal applied on a respective word line corresponding to each generated address (So, col. 4, lines 52-59; col. 5, lines 7-12; Fig. 1, element 16); *It should be noted that the "clock input circuit" is analogous to the "clock signal generator."*

and a bit line voltage generator for generating a bit line voltage applied on a respective at least one bit line corresponding to each generated address (So, col. 5, 39-46, and 56-60; Fig. 3, element 31). *It should be noted that the "high frequency waveform means" is analogous to the "bit line voltage generator." Also, see the citation note for claim 4 above.*

17. **As per claim 15**, the combination of So/Okazawa discloses the address generator generates a respective binary bit pattern for each of the addresses, and wherein the gray code converter converts the respective binary bit pattern to a

respective gray code bit pattern for each of the addresses (Okazawa, col. 3, lines 35-44; Fig. 1, elements 1 and 2), and wherein the system further comprises:

address decoders for decoding the respective gray code bit pattern for accessing the memory device for determining the respective at least one memory cell to have the stressing signals applied thereon (So, col. 6, lines 46-50; Okawaza, col. 3, lines 44-46). *It should be noted that in the combined invention of So/Okawaza, Okawaza's grey code address would be output to So's address decoders for high frequency testing.*

18. **As per claim 17**, the combination of So/Okazawa discloses means for cycling through the respective bit pattern for each of the addresses with a transition of a fixed number of bits for sequencing to each subsequent address (Okazawa, col. 5, lines 9-11 and 53-67; Fig. 4). *It should be noted that pg. 12, lines 27-29 of Applicant's specification appear to define this means as a "binary to gray code converter." Okazawa's "binary/grey conversion logic circuit" is equivalent to Applicant's "binary to gray code converter." Also, see the citation note for claim 7 above.*

19. **As per claim 18**, the combination of So/Okazawa discloses the memory device is a flash memory device (So, col. 3, lines 51-55).

20. **As per claim 19**, the combination of So/Okazawa discloses the signal generators include:

a clock signal generator for generating a clock signal applied on a respective word line corresponding to each generated address (So, col. 4, lines 52-59; col. 5, lines 7-12; Fig. 1, element 16); *See the citation note for the similar limitation in claim 14 above.*

and a bit line voltage generator for generating a bit line voltage applied on a respective at least one bit line corresponding to each generated address (So, col. 5, 39-46, and 56-60; Fig. 3, element 31). *See the citation notes for the similar limitations in claims 4 and 14 above.*

21. **Claims 6, 10, 16, and 20 are rejected under 35 U.S.C. 103(a) as being obvious over So in view of Okazawa as applied to claims 1 and 10 above, and in further view of Gouravaram et al. (U.S. Patent 5,872,449).**

22. **As per claims 6, 10, 16, and 20**, the combination of So/ Okazawa discloses all the limitations of claims 6, 10, 16, and 20 except heating the memory device during the predetermined stress time period for HTOL (high temperature operating life) testing of the memory device.

Gouravaram discloses heating the memory device during the predetermined stress time period for HTOL (high temperature operating life) testing of the memory device (col. 3, line 39 – col. 4, line 6; col. 4, line 62 – col. 5, line 17; Fig. 3). *It should be noted that the "memory circuits 30 a-d" are analogous to the "memory device."*

The combination of So/Okazawa and Gouravaram are analogous art because they are from the same field of endeavor, that being systems for testing memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Gouravaram's HTOL test with So/Okazawa's stress testing system.

The motivation for doing so would have been to simplify failure analysis during qualification testing (Gouravaram, col. 1, lines 38-41).

Therefore, it would have been obvious to combine So/Okazawa and Gouravaram for the benefit of obtaining the invention as specified in claims 6, 10, 16, and 20.

Response to Arguments

23. Applicant's arguments with respect to **claims 1-20** have been considered but are moot in view of the new grounds of rejection.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-20** have received a second action on the merits and are subject of a second action final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,276,647 (Matsui et al.) discloses static random access memory including stress test circuitry.

2. U.S. Patent 5,375,091 (Berry Jr. et al.) discloses a memory embedded in a integrated processor chip that is dynamically stressed tested by repeatedly writing a test pattern to the data locations of the memory in which a high percentage of the memory cells are sequentially written with complementary data in order to create a high stress on the memory devices.

3. U.S. Patent 5,570,317 (Rosen et al.) discloses stress circuitry for detecting data retention defects in the memory cells.

4. U.S. Patent 6,894,937 (Garni et al.) discloses a circuit that provides a stress voltage to magnetic tunnel junctions (MTJs), which comprise the storage elements of a magnetoresitive random access memory (MRAM), during an accelerated life test of the MRAM.

5. U.S. Patent 6,965,526 (Cavaleri et al.) discloses sectored flash memory comprising means for controlling and for refreshing memory cells.

6. U.S. Patent 7,076,710 (Knips et al.) discloses a Method and system for testing a memory array having a non-uniform binary address space.

7. U.S. Statutory Invention Registration H001741 (Cruts) discloses a method and apparatus for pattern sensitivity stress testing of memory systems.

8. Hakenes et al., "A Segmented Gray Code for Low-Power Microcontroller Address Buses", 1999, Proceedings of the 25th EUROMICRO Conference, IEEE, pp. 1-4 discloses switching activity reduction when using Gray code.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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